CLAIMS

[0061] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An image sensor pixel cell comprising:

a gate stack formed over a substrate of a first conductivity type;

an implanted well region of said first conductivity type located below at least a portion of said gate stack and extending to one side of said gate stack; and

a photo-conversion device laterally displaced from said implanted well region on an opposite side of said gate stack from said implanted well region.

2. The pixel cell of claim 1, wherein said implanted well region is located below about half the channel length of said gate stack.

3. The pixel cell of claim 1, wherein said implanted well region is further located below at least a portion of an isolation region of said pixel.

4. The pixel cell of claim 1, wherein said implanted well region has an implant dose of about 5×10^{11} to about 5×10^{13} atoms per cm^2.

5. The pixel cell of claim 4, wherein said implanted well region has an implant dose of about 1 x 10^{12} to about 5 x 10^{12} atoms per cm^2.

6. The pixel cell of claim 1, wherein said implanted well region has a depth below said gate stack of about 4,000 to about 40,000 Angstroms.

7. The pixel cell of claim 6, wherein said implanted well region has a depth below said gate stack of about 10,000 to about 30,000 Angstroms.

8. The pixel cell of claim 1, wherein said photo-conversion device is selected from the group consisting of a photoconductor, a photogate and a photodiode.

9. The pixel cell of claim 8, wherein said photodiode is a p-n-p photodiode

10. The pixel cell of claim 8, wherein said photodiode is and an n-p-n photodiode.

11. The pixel cell of claim 1, wherein said first conductivity type is p-type or n-type.

12. The pixel cell of claim 1, wherein said pixel is part of a CMOS imager.

13. The pixel cell of claim 1, wherein said pixel cell is a 3T pixel cell.

14. The pixel cell of claim 1, wherein said pixel cell is a 4T pixel cell.

15. The pixel cell of claim 1, wherein said pixel cell is a 5T pixel cell.

16. The pixel cell of claim 1, wherein said pixel cell is part of a CCD imager.

17. An isolation structure for a pixel sensor cell, comprising:

a dielectric material formed within a substrate; and

an implanted well region located below at least a portion of said dielectric material and laterally displaced from a region of a photo-conversion device.

18. The isolation structure of claim 17, wherein said implanted well region extends below the width of said dielectric material.

19. The isolation structure of claim 17, wherein said implanted well region has an implant dose of about 5×10^{11} to about 5×10^{13} atoms per cm^2.

20. The isolation structure of claim 17, wherein said implanted well region has an implant dose of about 1×10^{12} to about 5×10^{12} atoms per cm^2.

21. The isolation structure of claim 17, wherein said photo-conversion device is one of a photodiode, a photogate and a photoconductor.

22. The isolation structure of claim 17, wherein said dielectric material is part of an STI structure.

23. The isolation structure of claim 17, wherein said dielectric material is part of a LOCOS structure.

24. The isolation structure of claim 17, wherein said pixel sensor cell is part of a CMOS sensor.

25. The isolation structure of claim 17, wherein said pixel sensor cell is part of a CCD sensor.

26. A pixel structure comprising:

a charge collection region formed in a substrate;

an implanted well region of a first conductivity type formed in said substrate and laterally displaced from said charge collection region by about 200 Angstroms to about 5,000 Angstroms, said charge collection region being of a second conductivity type; and

a second doped layer of said first conductivity type located above said charge collection region.

27. The pixel structure of claim 26, wherein said implanted well region extends below at least a portion of a gate of a transfer transistor formed over said substrate, said transfer gate transferring charge accumulated in said charge collection region to a doped region of said second conductivity type.

28. The pixel structure of claim 27, wherein said implanted well region is laterally displaced from said charge collection region by about half the channel length of said gate.

29. The pixel structure of claim 26, wherein said implanted well region is doped with a p-type dopant at an implant dose of about 5 x 10^{11} to about 5 x 10^{13} atoms per cm^2.

30. The pixel structure of claim 27, wherein said implanted well region has a depth below said gate of said transfer transistor of about 4,000 to about 40,000 Angstroms.

31. The pixel structure of claim 26, wherein said first conductivity type is p-type and said second conductivity type is n-type.

32. The pixel structure of claim 26, wherein said first conductivity type is n-type and said second conductivity type is p-type.

33. The pixel structure of claim 26, wherein said implanted well region is part of a CMOS sensor.

34. The pixel structure of claim 26, wherein said implanted well region is part of a CCD sensor.

35. An image sensor comprising:

a substrate;

a transistor transfer gate formed over said substrate;

an isolation region formed within said substrate;

a p-type implanted well located below at least a portion of an active area of said transistor transfer gate and below at least a portion of said isolation region;

a p-n photodiode laterally displaced from said p-type implanted well and comprising a p-type surface layer and an n-type doped layer located adjacent and below said p-type surface layer; and

a floating diffusion region provided in said p-type implanted well to receive charges gated by said transfer gate.

36. The image sensor of claim 35, wherein said p-type implanted well extends to about half the length of said transistor gate.

37. The image sensor of claim 35, wherein said p-type implanted well extends below said isolation region.

38. The image sensor of claim 35, wherein said image sensor is a CMOS image sensor.

39. The image sensor of claim 35, wherein said image sensor is a CCD sensor

40. A CMOS imager system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor, said CMOS imaging device comprising:

a gate stack formed over a substrate;

an implanted well region of a first conductivity type located below at least a portion of said gate stack; and

a pixel laterally displaced from said implanted region by about 200 Angstroms to about 5,000 Angstroms.

41. The system of claim 40, wherein said implanted well region extends to about half the length of said gate stack.

42. The system of claim 40, wherein said implanted well region further extends below at least a portion of an isolation region adjacent said pixel.

43. The system of claim 40, wherein said implanted well region has an implant dose of about 5×10^{11} to about 5×10^{13} atoms per cm^2.

44. The system of claim 40, wherein said pixel comprises a photosensor.

45. The system of claim 44, wherein said photosensor is one of a photoconductor, a photogate and a photodiode.

46. The system of claim 45, wherein said photodiode comprises a surface layer of said first conductivity type, and a doped region of a second conductivity type located below said surface layer and relative to said pinned layer.

47. The system of claim 46, wherein said first conductivity type is p-type and said second conductivity type is n-type.

48. The system of claim 46, wherein said first conductivity type is n-type and said second conductivity type is p-type.

49. The system of claim 46, wherein said photodiode is one of a p-n-p photodiode and an n-p-n photodiode.

50. A 4T pixel sensor cell comprising:

a substrate of a first conductivity type;

an implanted well region of said first conductivity type formed within said substrate and located below at least a portion of a transfer gate of a transfer transistor, said implanted region further comprising:

a floating diffusion region provided within said implanted well region to receive charges gated by said transfer gate;

first source and drain regions of a reset transistor formed over said substrate;

second source and drain regions of a source follower transistor; and

third source and drain regions of a row select transistor.

51. The pixel sensor cell of claim 50, wherein said implanted well region extends to about half the channel length of said transfer gate.

52. The pixel sensor cell of claim 50, wherein said implanted well region has an implant dose of about 5×10^{11} to about 5×10^{13} atoms per cm^2.

53. The pixel sensor cell of claim 52, wherein said implanted well region has an implant dose of about 1 x 10^{12} to about 5 x 10^{12} atoms per cm^2.

54. The pixel sensor cell of claim 50, wherein said implanted well region has a depth below said transfer gate of about 4,000 to about 40,000 Angstroms.

55. A method of processing an implanted region, comprising:

forming at least one transistor gate over a substrate of a first conductivity type;

forming an implanted well region of said first conductivity type below at least a portion of said transistor gate; and

providing an electrical device laterally displaced from said implanted region.

56. The method of claim 55, wherein said implanted well region is formed to a thickness of about 4,000 to about 40,000 Angstroms.

57. The method of claim 55, wherein said implanted well region is formed below about half the channel length of said transistor gate.

58. The method of claim 55, wherein said implanted well region is formed by conducting an implant with dopants of said first conductivity type in an area of said substrate below half the channel length of said transistor gate.

59. The method of claim 55, wherein said implanted well region has an implant dose of about 5 x 10^{11} to about 5 x 10^{13} atoms per cm^2.

60. The method of claim 55, wherein said electrical device is an imager.

61. The method of claim 60, wherein said electrical device is a CMOS imager.

62. The method of claim 60, wherein said electrical device is a CCD imager.

63. The method of claim 60, wherein said electrical device is a photosensor, a photodiode, a photoconductor or a photogate.

64. A method of forming a photodiode for a pixel sensor cell, comprising:

forming at least one isolation region in a substrate;

forming a gate stack over said substrate;

forming an implanted well region of a first conductivity type in said substrate and adjacent at least a portion of said isolation region and of said gate stack;

forming a doped region of a second conductivity type in said substrate and laterally displaced from said implanted well region; and

forming a doped layer of said first conductivity type in said substrate, said doped layer being in contact with said doped region of said second conductivity type.

65. The method of claim 64, wherein said implanted well region is formed below at least a portion of said isolation region.

66. The method of claim 64, wherein said implanted well region is formed below about half the channel length of said gate stack.

67. The method of claim 64, wherein said doped region of said second conductivity type is laterally displaced from said implanted well region by about 1,000 Angstroms to about 5,000 Angstroms.

68. The method of claim 67, wherein said doped region of said second conductivity type is laterally displaced from said implanted well region by about 1,000 Angstroms to about 3,000 Angstroms.

69. The method of claim 64, wherein said implanted well region is implanted with a p-type dopant and an implant dose of about 5×10^{11} to about 5×10^{13} atoms per cm^2.

70. The method of claim 64, wherein said implanted well region is formed to a thickness of about 4,000 to about 40,000 Angstroms.

71. The method of claim 64, wherein said implanted well region is formed subsequent to the formation of said gate stack.

72. The method of claim 64, wherein said implanted well region is formed prior to the formation of said gate stack.

73. The method of claim 64, wherein said gate stack is part of a transfer transistor.

74. The method of claim 64, wherein said gate stack is part of a reset transistor.

75. The method of claim 64, wherein said photodiode is a p-n photodiode or an n-p photodiode.

76. The method of claim 64, wherein said photodiode is part of a CCD sensor.

77. The method of claim 64, wherein said photodiode is part of a CMOS sensor.

78. A method of forming a p-n photodiode for a CMOS imaging device, said method comprising:

forming at least one trench isolation region in a silicon substrate;

forming a gate stack of a transistor over said silicon substrate; and

forming a doped well region below about half the channel length of said gate stack and below said trench isolation

region by implanting p-type ions in said silicon substrate, said doped region having an implant dose of about 5 x 10^{11} to about 5 x 10^{13} atoms per cm^2.

79. The method of claim 78 further comprising the steps of:

forming an n-type doped region in said silicon substrate; and

forming a p-type doped layer in said silicon substrate and above said n-type doped region, said p-type doped layer and said n-type doped region being laterally displaced from said doped well region.

80. The method of claim 79, wherein said n-type doped region is laterally displaced from said doped well region by about half the channel length of said gate stack.

81. The method of claim 78, wherein said doped well region is formed below about half the channel length of said gate stack.

82. The method of claim 78, wherein said doped well region is formed to a thickness of about 4,000 to about 40,000 Angstroms.